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Optimized Inter Real-Time Simulator Communication Utilizing Transmission Line Delay Variety

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Abstract. Hardware-in-the-loop (HIL) testing based on real-time simulators is one of the critical methods for the power system and the power electronics system research. Using multiple interconnected simulators to enhance parallel computing performance is a common method. However, with the increasing demand for enlarging system scale and shortening simulation time-step, more dedicated communication resources and a higher amount of transferred data are required. This paper proposed a method for optimizing inter real-time simulator communication utilizing the delay variety of the distributed transmission line model, which can reduce the communication hardware resources and increase the data throughput with no loss of the simulation accuracy. In the case study of a system containing 100 wind turbines and 20 sets of IEEE 39-bus system on four real-time simulators, the communication resource consumption is reduced by 48.78% with the proposed optimization method.

Key words. Real-time Simulator, Transmission Line Model, Communication Optimization

1. Introduction

The large-scale utilization of renewable energies and power electronics converters imposes significant challenges to the safe and stable operation of the modern power system. Electromagnetic transient simulation and real-time simulation are important tools in the design, testing, and operation of the power system [1]-[2].

Due to the increment of the system scale and the switching frequency of power electronic devices, higher computational capability and smaller simulation time-step are required [3]. Applying multiple interconnected simulators is a common method to enhance the simulation performance for large-scale systems [4]-[6]. With the decoupling characteristics of the distributed parameter transmission line model, the power system can be separated into multiple subsystems allocating to different simulators for parallel computing [7]. It requires strict real-time data exchange between simulators at the microsecond level for each time step. To ensure stable data transmission with fixed intervals and adequate flexibility, field programmable gate arrays (FPGAs) are often used for communication between simulators [8]-[10].

With conventional inter real-time simulator communication, the data exchange latency is typically equal to one simulation step. If the inherent traveling wave delay of long transmission lines exceeds the communication latency, a longer data exchange latency which can be multiple simulation time-step has no impact on the accuracy of the simulation results [11]. Therefore, it is not necessary to constrain the data exchange latency within one simulation time-step for all transmission line models used for network decoupling. Relaxed latency requirement provides the foundation for communication process optimization. Based on the above idea, this paper proposed an optimized inter real-time communication method that uses multiple data exchange modules with different communication latencies corresponding to the various transmission line distances.

This work first introduced the principle of the distributed parameter transmission line model. Then the proposed optimization method and its implementation were described. A case study of a power system containing 100 wind turbine models and 20 sets of IEEE 39-bus systems was simulated on the platform composed by 4 real-time simulators. The FPGA resource usage was reduced by 48.78% after applying the proposed communication optimization method. Equivalently, with the same amount of resources, the amount of the exchanged data can be higher. Besides the real-time simulation, the proposed method is also applicable for

general electromagnetic transient simulation using multiple computers.

2. Communication Optimization Based on Transmission Line Delay Variety

A. Principle of Transmission Line Delays and Network Decoupling

The Bergeron line model is commonly used in the electromagnetic transient simulation for the long-distance transmission line with distributed parameters [12]-[13], as illustrated in Fig. 1.

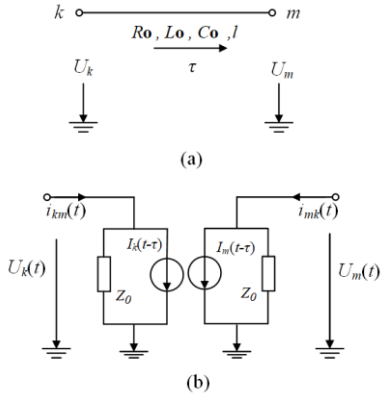

Fig. 1. Bergeron line model schematic: (a) distributed line parameters (b) circuit model schematic

In Fig. 1, R_0, L_0, and C_0 denote the resistance, the inductance, and the capacitance per unit length respectively. The total length of the line is l, and the wave impedance is Z_0. At the sending end, the voltage and the current are represented as $U_k(t)$ and $i_{km}(t)$, while at the receiving end, they are denoted as $U_m(t)$ and $i_{mk}(t)$. The time delay τ of the traveling wave propagating from the sending end to the receiving end can be expressed as:

$$\tau = \frac{l}{v}, \tag{1}$$

or equivalently:

$$\tau = l\sqrt{L_0 C_0}, \tag{2}$$

where v represents the propagation speed with the unit of m/s, τ is the propagation time with the unit of s, and l is the transmission line length with the unit of m.

The terminal current can be calculated as follows:

$$\begin{cases} i_{km}(t) = \dfrac{1}{Z_0}U_k(t) + I_k(t-\tau) \\ i_{mk}(t) = \dfrac{1}{Z_0}U_m(t) + I_m(t-\tau) \end{cases}, \tag{3}$$

where $I_k(t-\tau)$ and $I_m(t-\tau)$ are the historical current sources.

The model utilizes the characteristic of traveling wave propagation delay, employing historical current sources from the other side at one or several simulation time steps prior, thus the solution is not influenced by the node voltages of the other side at the current simulation time [14]. Since a large amount of transmission lines exist in the power system, the characteristic is well-suited for decoupling the simulated system into multiple sub-networks with no error introduced. Then the computation tasks of the sub-networks can be allocated into several or several tens of real-time simulators for parallel computing.

B. Communication Optimization with Various Latencies

In a power system, transmission line distance can span from several tens to hundreds of kilometers, which corresponds to the traveling wave delays from tens to hundreds of microseconds, as derived from Equations (1) and (2). Conventional inter-simulator communication restrains the latency within one time-step or fixed multiple time-steps, which can lead to the following issues:

1) *High FPGA resource consumption*: Due to the single-step restraint, the required FPGA resources are much higher when implemented with full parallelism. Besides communication tasks, the FPGA resources may be also used for circuit computations tasks, such as the calculation of modular multi-level converters or power electronics converters. Therefore it is necessary to reduce the hardware resource consumption to lower the overall cost.
2) *Communication capacity limitation*: For large-scale system simulation, a fixed single-step latency can restrict the data throughput, especially when the interconnected simulators increase significantly.

To address the above issues, the communication module optimization method based on the inherent delay varieties among transmission lines is proposed. Multiple communication modules with various transmission latencies are implemented avoiding full parallelism design for all data. The exchanged history data for various transmission lines can go through appropriate modules.

The key concept is relaxing the latency restraint to reduce the FPGA latency requirement without affecting the simulation accuracy. It is noted that the distance of the power system transmission line is correlated to the inter-communication latency or the equivalent digital transmission line distance.

C. Design Implementation

To realize the proposed method, the inter-changed data are first categorized into three groups: low-latency, medium-latency, and high-latency. In the demonstrating design, they correspond to the one time-step, the two time-steps, and the above two time-steps. For each simulator, the exchanged data are sequenced from low

latency to high-latency and are transmitted through an optical fiber link with Aurora protocol.

The switch dedicated for inter real-time simulator communication is implemented on the FPGA with High-Level Synthesis (HLS) design methodology [15]-[17]. It uses C-style code instead of Hardware Design Language (HDL), which can significantly reduce the design effort. Furthermore, by simply applying directives in code, it can realize multiple hardware designs with different resource consumptions and latencies. The directive 'UNROLL' is used to fully flatten the loop for parallelized design with minimal latency. The directive 'PIPELINE' normally can used in the design with lower hardware consumption. The three communication modules with low, medium, and high latencies are implemented by applying various combinations of the directives.

The exchanged data volume and routes in the three categories are known and remain unchanged through the simulation. Therefore it is unnecessary to add the data frame head. Instead, the above information is set as the configuration for the switch before the simulation begins.

The switch implements the following three major steps during each time-step.

1) Receive the data pack and disassemble it into three parts according to the latency information.
2) Execute the data exchange for the three switch modules simultaneously.
3) Reassemble the data pack for each channel and send the data pack to the simulators. The data sent back are not necessarily from the same simulation step.

The above modules can be synthesized as IP cores shown in Fig. 2.

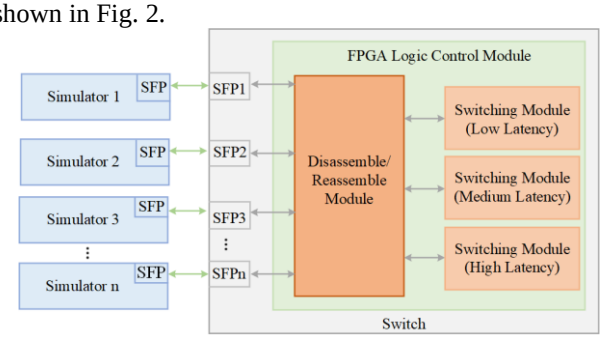

Fig. 2 System block diagram

Although using three switch modules, the overall design resources can be lower due to the resource optimization for the ones with higher latency.

From the other perspective, the data volume requiring one time-step delay is smaller. The switch no longer needs to process the complete data queue but only for the ones requiring one step delay, which leads to smaller latency. In such a case, the simulation time-step can be lowered as long as the simulator satisfies the timing requirement. The smaller time-step is helpful since it corresponds to a small transmission line distance for network decoupling, which commonly exists in wind farms. To realize the real-time simulation with a very small time-step, FPGA is one of the commonly used platforms. Therefore, saving the hardware resources in the communication part is valuable.

3. Case Study

A. Simulation Platform

The real-time simulation platform is composed by four DONGJU® real-time simulators [18], inter connected by the switch using the FPGA as shown in Fig. 3.

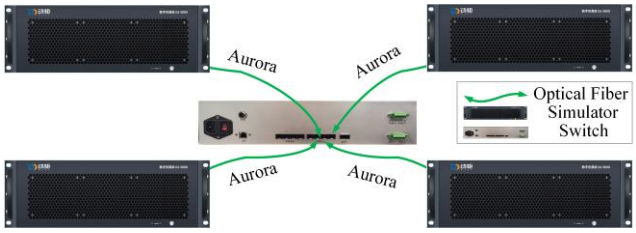

Fig. 3 Simulation platform schematic

The system composed of 20 sets of IEEE 39-bus system and 100 wind turbines in total are simulated on the platform, with the simulation time step of 10μs. The case study is designed to demonstrate the effectiveness of the proposed communication optimization method. All parts are interconnected by Bergeron transmission line models, illustrated in Fig. 4. The first and the fourth simulators each run 10 sets of the IEEE 39-bus system, and there are 50 interconnected transmission lines, which corresponds to 150 double-precision floating-point variables in each direction of the communication. The second and the third simulators each run 50 wind turbine models with the control systems. The IEEE 39-bus system is also connected with the wind turbines by the transmission line model, which requires another 300 variables in both directions among the simulators.

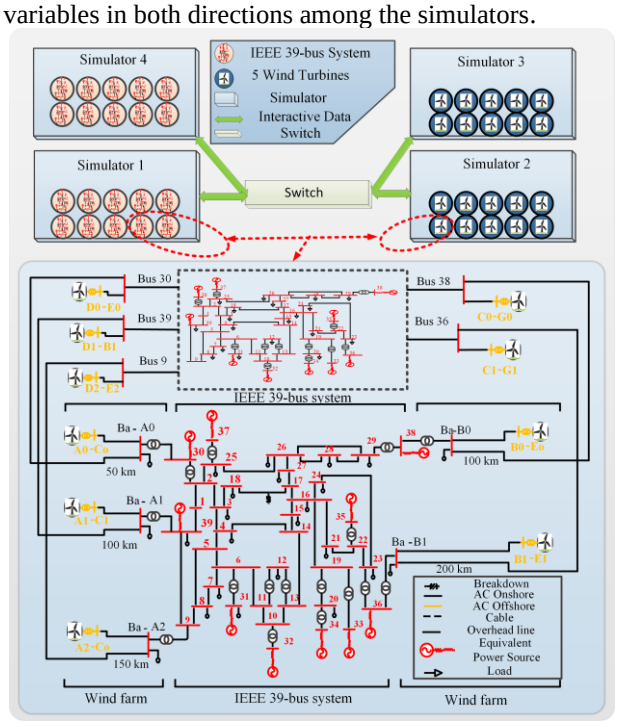

Fig. 4 Partition and the communication of the case study

In total, 900 bi-directional variables are processed in the switch during each time-step.

B. Resource Consumption

The FPGA resource comparison between the conventional communication method and the proposed optimization scheme was conducted. Table I summarized the resource usage based on Xilinx Kintex-7 XC7K420T-2L (FFG901) FPGA, including the look-up-tables (LUTs) and flip-flops (FFs).

After the optimization, both the consumption of LUTs and FFs were nearly halved.

Table I. - Resource Consumption Before and After Optimization

Resource Type	Usage Before Optimization	Usage After Optimization
LUT	52729(20.23%)	26555(10.19%)
FF	284082(54.51%)	145500(27.92%)

The result demonstrated the merit of the proposed communication optimization method in the aspect of resource consumption reduction. The reduction rate can be higher when more simulators connected together to simulate a lager power system.

C. Simulation Results

This section presented some of the simulation results demonstrating that the proposed method introduces no errors. A fault was applied at the gird side closed to a wind turbine at the time instance of 2 second, which lasted for 0.1 second. The transient responses of the wind turbine system, including DC voltage, active power, reactive power, and instantaneous current are presented in Fig. 5 and Fig. 6.

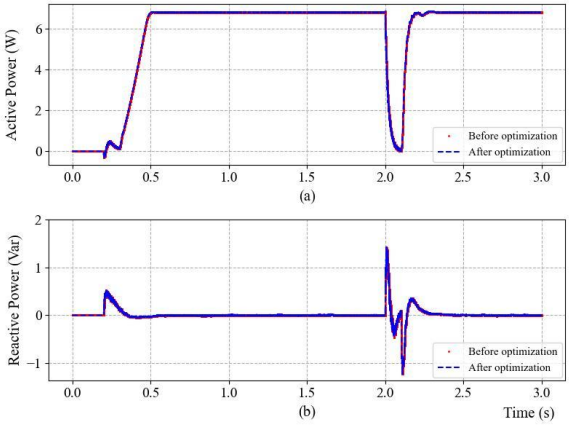

Fig. 5 Transient waveforms of active and reactive power before and after the optimization:(a) active power (b) reactive power

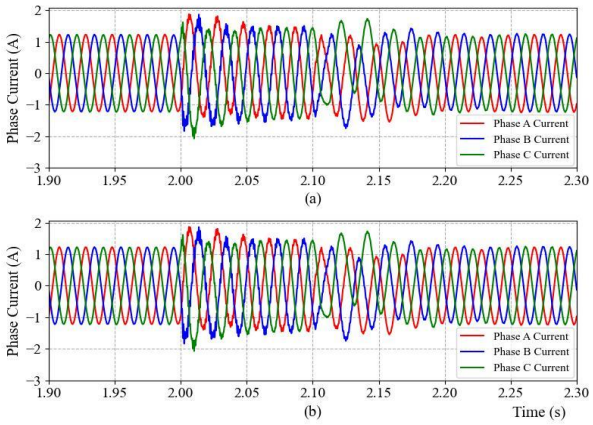

Fig. 6 Transient waveforms of the current before and after the optimization: (a) phase current before optimization (b) phase current after optimization

In Fig. 5, active power dropped sharply due to the fault and then recovers. There was a spike of reactive power at the beginning of the transient due to the voltage drop. Fig. 6 presented the three-phase instantaneous current waveforms which oscillate after applying the fault. As shown in Fig. 5 and Fig. 6, the results matched well before and after applying the proposed optimization method.

4. Conclusion

To increase the efficiency of the inter real-time simulator communication, this work proposed an optimization method based on the traveling wave delay variety of the Bergeron transmission line model in electromagnetic transient simulation. The design implementation on FPGA was described, and a case study composed of the power grid and the wind turbines on the real-time simulation platform was conducted. The FPGA hardware resource was halved after applying the proposed method without compromising the simulation accuracy. The proposed method is applicable to various practical power system topologies with long transmission lines. It is expected that the communication resource reduction rate can be higher for larger system scale interconnecting more simulators, which can be validated in future work.

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