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Robust power converters for renewable generation systems in future networks with short circuit ratio wide variations

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Abstract. The European Directive (EU) 2018/2001 requests the connection of a new renewable inverter-based resources (RIR) but ensuring that the connection point is strong enough to minimize and avoid possible interaction phenomena. Historically, the indicator used to determine the strength of a network has been the Short Circuit Ratio (SCR). Until now, the tendency had been to ensure that the network remained strong enough with High SCR, but another possibility is to ensure that RIR can operate stably and reliably at different SCR values, both high and low. The inverters currently deployed in European power systems use grid following inverter technology (GFI). The main objective of the present work is the redesign of the traditional current regulators of JEMA Energy PV family inverters, based on grid following technology, to guarantee the stability of electrical systems with a variable short-circuit ratio in the range [1÷20]. To achieve this, the current loops of the inverter are redesigned, introducing an additional first-order controller that improves the dynamics of the system and allows stable and efficient behaviour. For validation purposes, the system is analysed under adverse fault scenarios. The results obtained in all cases are satisfactory, but the stability with PLL (phase lock loop) slower than those originally used, is better.

Key words. Renewable power converters, Grid following converters, robustness, SCR, weak and strong grid, fault events, UE 2016/631.

1. Introduction

Directive (EU) 2018/2001 of the European Parliament establishes a binding global target for the Union to achieve a minimum share of 32% of energy from renewable sources in the Union's gross final energy consumption by no later than 2030. To achieve this target, the generation mix in European power systems is shifting away from synchronous machines toward renewable inverter-based resources (RIR). As a result, the firmness of the network may be compromised.

Historically, the Short Circuit Ratio index (SCR) has been the most widespread indicator to calculate the strength of the power system (ability to respond to variations in active and reactive power). The SCR is defined as the relationship between the short circuit power at the connection point and the nominal power of the RIR connected to it.

Red Eléctrica de España (REE), in its document "Technical criteria for evaluating network strength for integration of electric park modules according to existing technical literature" [1] establishes that a network is considered weak regarding the connection of a certain RIR when SCR<5, or very weak, when SCR<3 in a High Voltage node. In these cases, the power system is more sensitive to injections of active and/or reactive power and, therefore, the connection of a new RIR can complicate its stability (failures to withstand voltage dips, interaction between controls, instabilities in controls, etc.).

However, a network is considered strong with SCR>5 so the power system is more unaffected by changes in active and/or reactive power and with less tendency to instabilities.

When requesting the connection of a new electrical RIR, it must be guaranteed that the connection point is strong enough to minimize and avoid possible interaction phenomena. But another possibility is to ensure that RIR can operate stably and reliably at different SCR values, both high and low of SCR values. The latter is the case analysed here.

The inverters currently deployed in European power systems use grid following inverter technology (GFI), meaning they react to or follow changes occurring in the grid and then try to inject real and reactive power to "follow" the voltage.

A safe and efficient energy transition requires that existing and future RIRs maintain grid stability conditions. For this reason, the controls implemented in GFIs must be robust enough to ensure a correct behaviour to wide ranges of SCR variation at their connection point.

The controllers of GFIs can produce line currents in phase (or not) with respect to the phase-to-neutral voltages. The amplitude of the currents and the phase difference are determined by the control signal, and they are limited by the passive elements of the LCL input filter, the grid impedance, the dc bus voltage, the maximum bearable power by the converter and the control signal, see [2].

The main objective of the present work is the redesign of the traditional current regulators of JEMA Energy PV family inverters, based on grid forming technology, to guarantee the stability of electrical systems with a variable short-circuit ratio in the range [1÷20]. The dynamic behaviour of the developed control will also be evaluated against the fast current injection requirements established in the Spanish ministerial order TED/749/2020.

A model of a JEMA photovoltaic inverter has been created in Matlab/Simulink equipped with the control algorithms implemented in real devices. The original control scheme of the converters is shown in Figure 1. This control scheme meets the requirements to respond to the TED/749/2020 regulation with high SCRs and respond to the requirements for rapid current injection during the faults.

In steady state, the system will execute the MPPT algorithm (not implemented in the study presented here) and will regulate the DC bus voltage and the reactive power injected into the grid. When a disturbance occurs, the MPPT algorithm will stop executing and the system will implement the fast current injection requirements contained in the TED/749/2020 standard. A detailed description of these requirements can be found in the wording of the standard itself in the BOE-A-2020-8965 [3]. However, we will summarize the main aspects here:

- In the presence of faults, the photovoltaic inverter must be capable of injecting/absorbing a positive sequence reactive current, in the case of balanced faults, and positive and negative sequence currents, in the presence of unbalanced faults.
- The magnitude of the positive sequence current will be defined by the positive sequence voltage error based on a positive sequence current control gain, K1, and by the current saturation limits that are defined, as indicated in Figure 8.a of document BOE-A-2020-8965.
- In the same way, the magnitude of the negative sequence current will be defined by the negative sequence voltage error based on a positive sequence current control gain, K2, and by the current saturation limits that are defined, also defined in Figure 8.a of document BOE-A-2020-8965.
- The maximum response and establishment times for the positive sequence current are 50 ms, and 60 ms in the case of the negative sequence.

During the time that the rapid current injection mode is active, the DC bus voltage will be defined by the P-V characteristic of the photovoltaic array.

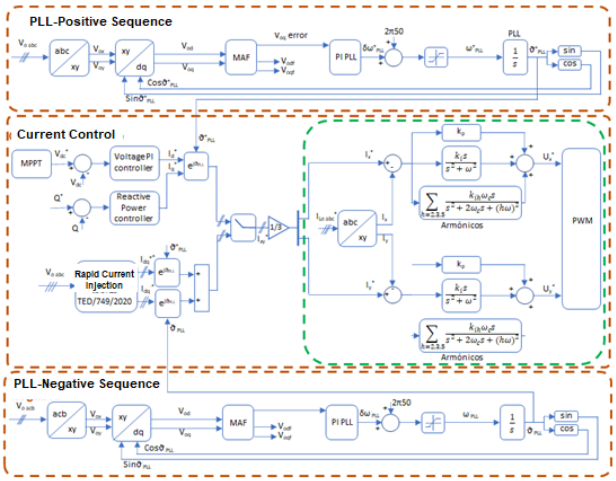

Fig.1. Original control block scheme.

2. Simulation Model

For the present study, the system chosen to be modelled is a 4400kW unit (Figure 3), whose technical characteristics are shown below:

- Nominal DC bus voltage = 1200Vdc (Maximum power voltage at 25ºC)
- Nominal RMS voltage at the converter output=670Vac
- Rated frequency of the network=50Hz
- Nominal current of the DC bus = Nominal DC Power / Nominal DC Voltage

-Rms Nominal Current = Nominal Power / sqrt (3) * phase to phase Nominal grid Voltage

The connection transformer also has been considered. Upstream of the connection transformer the faults are generated by impedances that act as a voltage divider causing the necessary fault in the grid, see Figure 2.

Initially and upstream of the grid transformer the grid voltage is imposed by the remote point voltage, V_Grid, and by the grid impedance, Z_Grid. If the converter does not inject current the voltage will be at the remote point voltage, V_Grid.

To cause a gap in the voltage, an impedance, Z_Fault, is introduced, which causes a voltage drop in the grid, leaving a residual voltage (V_residual) in the impedance, the higher the impedance the higher the residual voltage.

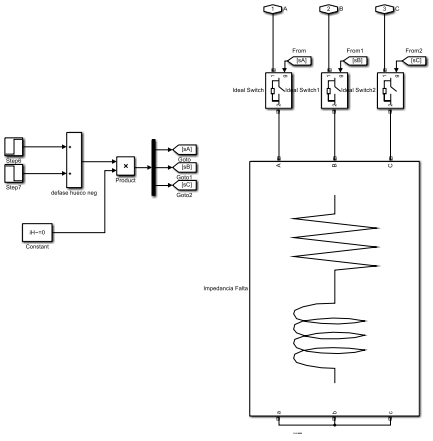

Fig.2. Model of Fault Generator.

The control system of the converter consists of a general control that takes care of the calculation of fast current injection setpoints. It receives the current setpoints in dq coordinates and is responsible for injecting them into the network.
The overall control consists of two main parts:
- Implementation of the fast current injection standard.
- Modification of setpoints to increase stability in case of SCR=1.

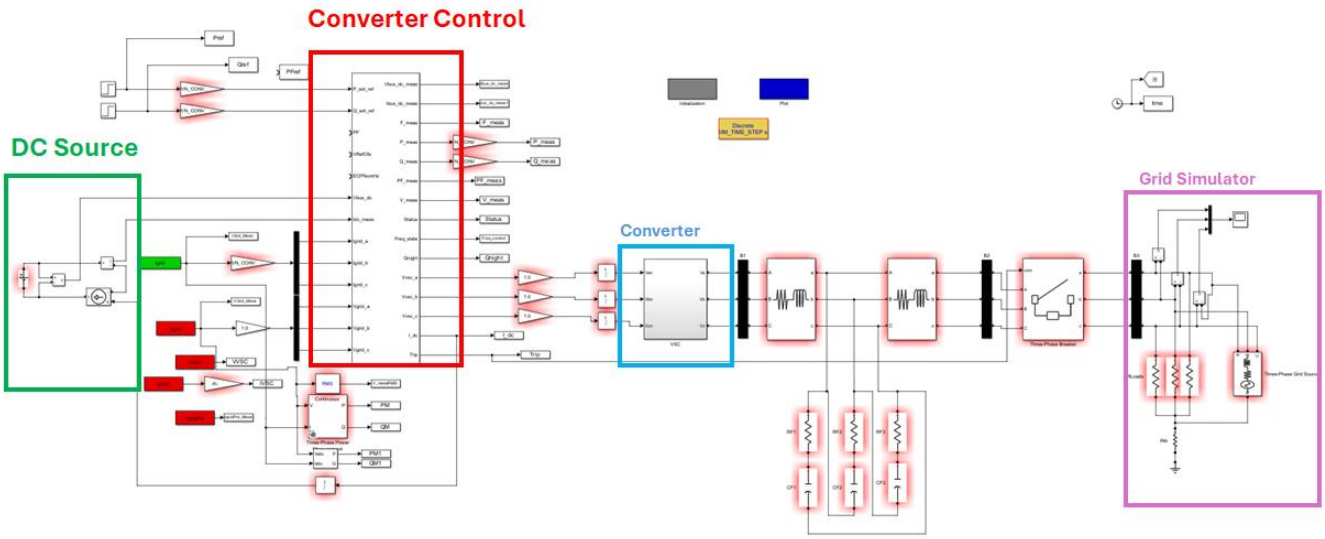

Fig.3. Simulink model of converter.

3. Controller Structure

To regulate the current, the control scheme using resonators in stationary αβ coordinates, see Figure 1. The structure is a double loop with cascaded controllers.
The control loops for α and β are identical, and are decoupled from each other, therefore the structure of the controller and the numerical value of its parameters will be the same in the two axes. The Figure 4 shows a general block diagram of the current control loop.

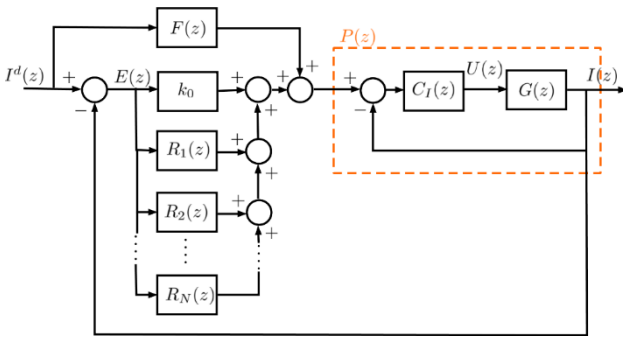

Fig.4. New Current Controller Schema with P(z)

The innermost loop is closed with a controller whose function is to attenuate the plant resonance and to ensure that the phase of the closed-loop transfer function of this first loop, P(z) given by equation (1), is maintained, as far as possible in the fourth quadrant. In other words, it is desirable that, at this frequency band in which the resonators are located, the regulator exercises great authority. For this purpose, the phase of P(z) should be kept between 0 and -90° since this way the phase assignment is more appropriate.

$$\boldsymbol{P(z) = C1(z)G(z)/(1 + C1(z)G(z))} \quad (1)$$

In the external control loop there are, in parallel, the proportional path k_0 and the resonators R_k (z), one for the fundamental frequency and the others for each of the harmonic frequencies to be treated.
The structure of each resonator (k-th resonator, R_k (z)) is shown in the attached Figure 5:

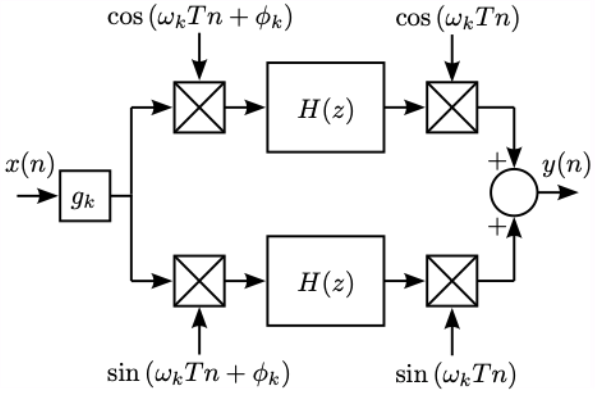

Fig.5. Resonant controller structure

Where H(z)=z/(z-1) is an integrator modelled after Backward Euler (zero relative degree) and g_k is the gain parameter of the resonator. The sinusoidal signals, without and with phase lag ϕ_k, are the carriers of the quadrature structure of the resonator that make the equivalent z-transfer function of the array to be:

$$R_k(z) = g_k \cdot \frac{\cos(\phi_k)z^2 - \cos(w_k T_s + \phi_k)z}{z^2 - 2\cos(w_k T_s)z + 1} \quad (2)$$

Importantly, the phase of the k-th resonator at its resonant frequency is:

$$\angle R_k(e^{j\omega_k T_s}) = -\phi_k) \quad (3)$$

Since the total open-loop transfer function is L(z)=(k_0+∑_k R_k (z))P(z), the choice of both ϕ_k and ϕ_k=∠P(e^(jω_k T_s)) maximizes the robustness of the design since, at resonator frequencies, one has that ∠L(e^(jω_k T_s))=0.

A. Controller Design

To assess that the design process of the controllers is adequate, certain indicators have been used, such as inner loop stability criteria, gain and phase margins, maximum absolute value of the closed-loop poles, norm-∞ of the sensitivity transfer function S(z)=1/(1+L(z)) and minimum distance of the polar curve of L(ω) to -1, d=1/(‖S‖_∞)) and also the graphic representation in the frequency domain.

The values of the resonator phases are calculated through equation (3) following the criterion of maximizing robustness as well as the values of the gains k_0 and g_k. For resonator gains, their value is decreasing with frequency so large values of g_k causes the amplitude of the frequency component corresponding to the k-th resonator to reach the desired value faster and vice versa. If the value of g_k is excessively large, then the amplitude of the frequency component corresponding to the k-th resonator is overshoot. This situation is not desirable because, during large amplitude transients, time responses with very strange and unsuitable profiles are produced.

On the other hand, it should be remembered that in the design of closed-loop control systems there is always a trade-off between higher response speed (higher bandwidth) and better performance and robustness. Therefore, it is necessary to reach a compromise between the two characteristics. Especially in the case of large parametric variations such as, for example, large variations in the SCR of the network, it is recommended to prioritize the robustness of the control loop against the temporal characteristics of performance.

The control algorithm operates at a sampling frequency F_s. The study analyses the worst case in which F_s is equal to the switching frequency (it would be more appropriate if it were at least twice that frequency.). In other words, in the frequency domain, the band available for the control loop ranges from 0 Hz to Fs/2 Hz. In order to meet the strict robustness requirements, the gain of the open loop transfer function, L(z), in the high frequency region must be much smaller than 1. Therefore, the frequency band in which the control loop has an important authority is quite small as can be seen in the Bode diagram of L(z).

Some graphical results corresponding to the designed controller are shown below, Figure 6, 7 and 8.

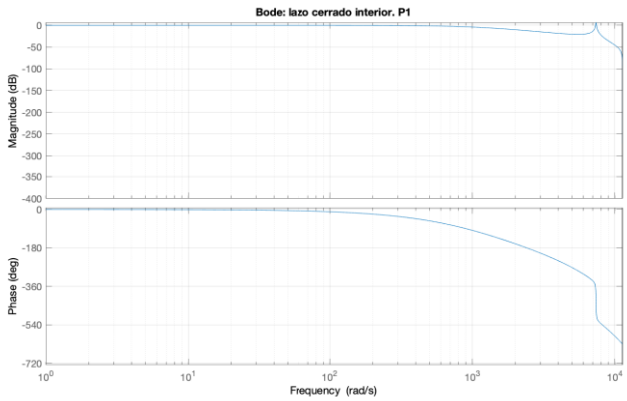

Fig.6. Bode of P(z), inner closed loop.

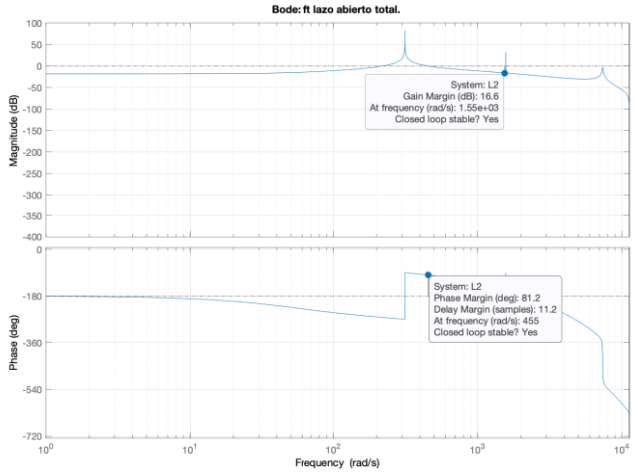

Fig.7. Bode of L(z), the open-loop transfer function of the system, with the values of the gain and phase margins

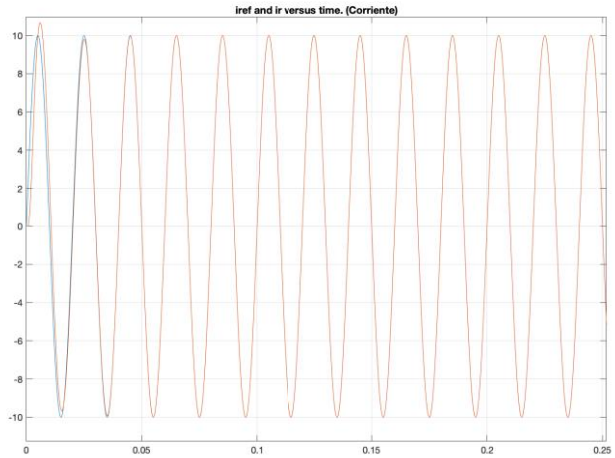

Fig.8. Temporal response of the closed-loop system (red signal) versus a sinusoidal reference (blue signal).

B. Results Validation

For the validation of the designed control system, the corresponding tests for compliance with voltage dips according to the " Norma técnica de supervisión de la conformidad de los módulos de generación de electricidad según el Reglamento UE 2016/631" [4], applicable in Spain under European guidelines. See table 49 of the

aforementioned document [4]. The results obtained are satisfactory, in all cases.

Figures 9 and 10 show the results obtained in two of the cases under study. One corresponds to a three-phase fault and the other to a two-phase fault. The three-phase fault case shown is of the U75TPmed type (three-phase fault of 75% depth) and the two-phase fault case is of the U75TPmed type (two phase fault of 75% depth), according to [2]. The pre-fault active power is 50% of the nominal power of the system, Pmed, in both cases.

In these Figures the output current in the reference frames dq, both positive and negative sequence, are plotted. These dq axes are measured according to a moving reference frame rotating at the nominal network frequency and are in phase with the voltage at the connection point. The scenarios in which the SCR is 1, 2, 5 and 10 have been plotted together. They are represented in p.u. values.

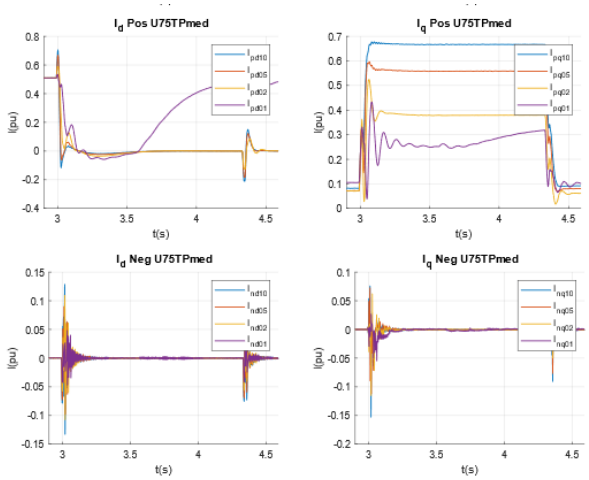

Fig.9. U75TPmed type: Positive current Id with SCR 1 (Ipd1), Positive current Iq with SCR 1 (Ipq1), Negative current Id with SCR 1 (Ind1), Negative current Iq with SCR 1 (Inq1), and those corresponding to SCR 2, 5 and 10 respectively (Ipd02, Ipq02, Ind02, Inq02, Ipd05, Ipq05, Ind05, Inq05, Ipd10, Ipq10, Ind10, Inq10).

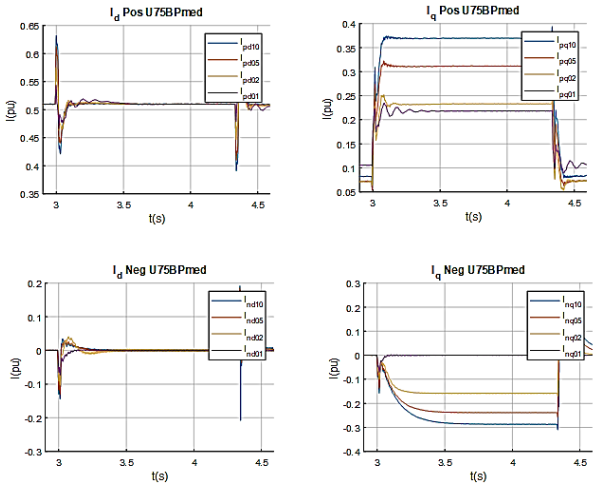

Fig.10. U75BPmed type: Positive current Id with SCR 1 (Ipd1), Positive current Iq with SCR 1 (Ipq1), Negative current Id with SCR 1 (Ind1), Negative current Iq with SCR 1 (Inq1), and those corresponding to SCR 2, 5 and 10 respectively (Ipd02, Ipq02, Ind02, Inq02, Ipd05, Ipq05, Ind05, Inq05, Ipd10, Ipq10, Ind10, Inq10).

4. Conclusion

In this project we have made adaptations to the control of Jema's converters to operate in a variable range of SCR from 1 to 20 network, trying to follow the previous control scheme and making the minimum possible changes in this one. It is likely that for working in low SCR environments the best option is to operate as Grid Forming converter, but this alternative has not been explored in the present study as it would imply a total change of the converter control and firmware.

The results obtained in all cases are satisfactory and the changes made to the control system have made it possible to work in very adverse scenarios. In the worst cases, for SCR=1, during a fault event, the system is very close to losing angular stability, so it is necessary to control the voltage at the point of connection in order not to lose system stability, so active setpoint increases must be done in a controlled manner.

In all cases the system is more stable with slower PLL than original ones (phase locked loop) which calculates the network frequency.

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